Large-Signal Model of Picosecond FET's and Measurement of the Step Response

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Abstract—**A FET large-signal model is developed for the time-domain CAD of ultrafast circuits. Numerical 2-D look-up tables describe the nonlinear parameters versus the device internal voltages. A dc and microwave FET characterization versus bias voltage followed by parameter extraction completely determines the tables of parameters. The model may be implemented in simulators handling 2-D tables and applied to commercial transistors without a detailed knowledge of the internal technology. The step response of a NEC710 MESFET is measured and compared with the model, demonstrating its accuracy in representing switching waveforms and transient phenomena in the range covering tens of picoseconds. The 20 ps switching time of the NEC710 shows that the presented methodology of modeling, measurement, and simulation is adequate for studying picosecond transient phenomena in single transistors.**

I. INTRODUCTION

THE PERFORMANCES of transistors available to the designer of high-speed circuits are improving at a fast pace and there is a growing need for large-signal models capable of accurately describing waveforms at picosecond scales. In the computer-aided design (CAD) of small-signal microwave circuits, a now standard and precise approach determines the parameters of the small-signal equivalent circuit at the bias conditions on the basis of dc and microwave measurements followed by parameter extraction [1], [2]. The design of nonlinear microwave circuits in the frequency domain uses large-signal models. The nonlinear elements may be represented by empirical analytical functions or polynomial expressions fitted with dc and S parameter measurements [2]. However these expressions become too complex to obtain good accuracy in the presence of strong nonlinearities and their systematic use in CAD would be too costly. The approach is mostly applied to the drain current characteristic in nonlinear microwave circuits [3]–[5].

In the CAD of high-speed digital circuits, the large-signal equivalent models have several nonlinear parameters which may vary over a wide range of values as a function of both drain and gate voltage biases. These elements are currently described with analytical expressions derived from an approximate physical description of the device. This modeling requires a knowledge of the device internal structure and of the manufacturing process, neither of which is available for commercial transistors. The models represent a trade-off between accuracy and simulation cost, and the description of nonlinear elements remains relatively crude. The simulations more often than not check circuit functioning rather than accurately describe signal waveforms. Several large-signal electrical models have been developed along the above lines for the time-domain simulation of fast circuits [6]–[8]. They have a moderate precision in the description of transient waveforms, and it may be said that accurate large-signal models of transistors at picosecond scales are presently lacking. Several table models have been proposed for MOS modeling at nanosecond scales in VLSI circuits [9]. Most of them are concerned with drain current modeling and are exploited for computing efficiency.

The prediction of accurate time-domain waveforms in circuits implemented with very fast transistors sets several conditions on the CAD approach:

a) an accurate electrical circuit model whose topology and elements describe precisely not only the static but also the dynamic properties through the nonlinear parameters (assuming the validity of the quasi-static approach);
b) the extraction of the model parameters with the bias voltage dependencies from static and high-frequency characterizations;
c) the efficient implementation of the electric model with its nonlinear parameter dependencies in a time simulator. In this last step, the implementation of the parameters may be done directly, i.e., numerically with data files, or with fitted analytical expressions. To our knowledge there is no published work along these lines related to modeling of transistors in the picosecond range.

We present a transistor large-signal model which answers to the above points for all nonlinear parameters. Its main original feature is the description of nonlinear elements with one-dimensional or two-dimensional numerical look-up tables as a function of the internal bias voltages of the transistor. The elements of the equivalent circuit are extracted from full dc, RF, and microwave small-signal device characterization in the $(V_{gs}-V_{ds})$ plane. Data on transistor technology, which are often proprietary, are unnecessary and the model may be applied to any commercial FET. We have first developed a MESFET model; preliminary results with a low-speed NEC3SK GaAs MESFET have been presented previously [10], [13]. We describe

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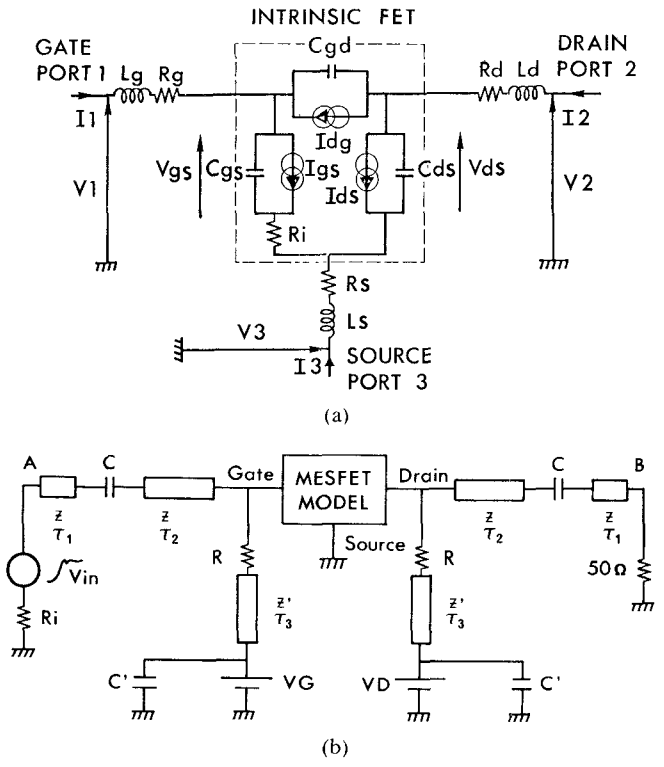

Fig. 1. Equivalent electric circuit. (a) Large-signal FET model. (b) Test card to measure NEC710 step response. The rectangles represent microstrip lines defined by their impedance and delay time ($Z = 50\ \Omega$, $t = 50$ ps, $t'' = 90$ ps, $Z' = 120\ \Omega$, $t' = 40$ ps). C and C' (100 pF) are dc and RF blocking capacitors, respectively; chip resistors value is $R = 510\ \Omega$.

here the capabilities of the model in the range covering tens of picoseconds with a detailed comparison of simulated and experimental step responses of the NEC710, a high-frequency GaAs MESFET. The methodologies of modeling, simulation, and measurement developed in the work have been validated for transistors with a 20 ps response time. The model and the information relating to the MESFET characterization are described in Section II. We present in Section III the experimental setup for measurement of the transistor step response. Section IV contains the measurement of the step response of the NEC710 and its analysis with simulation followed by a discussion of the transistor model.

II. Description of the Model

The large-signal equivalent circuit of the MESFET shown in Fig. 1(a) is evolved from the conventional small-signal equivalent circuit and the same notation is used [1], [2]. This relatively simple equivalent circuit assumes the validity of the quasi-static approximation as it neglects possible out-of-equilibrium phenomena. It is justified *a posteriori* by the measurements. The model is designed for strong nonlinear conditions such as determination of a step response and electronic sampling with operation in the ohmic part of the characteristic. Then all nonlinearities of the intrinsic device in the model are described as a function of the transistor drive voltages (V_{ds}, V_{gs}). The current sources I_{ds} and I_{gd} and the capacitances C_{gs}, C_{ds}, and C_{gd} depend on both bias voltages, V_{gs} and V_{ds}. The current source I_{gs}, representing the gate current with open circuit drain, describes the experimental characteristic of the FET input Schottky diode. The channel resistance R_i and the current source I_{gs} depend only on V_{gs}, as verified experimentally. The transistor access elements, the resistances R_g, R_d, and R_s, and the parasitic inductances L_g, L_d, and L_s are independent of bias conditions. For simplicity the circuit does not contain the respective electrode capacitances which are small relative to C_{gs}, C_{ds}, and C_{gd} (3–6 percent for NEC710) and are incorporated in the latter by the FET characterization with S-parameter measurements. There is no assumption relating to the device technological parameters beyond the implications of the equivalent circuit topology.

TABLE I
Small-Signal Model Parameters of NEC710 MESFET: Selected Bias Voltages Illustrate the Range of Variation of the Nonlinear Parameters

	Vds=1V		Vds=3V		
Element	Vgs=-1V	Vgs=0V	Vgs=-1V	Vgs=0V	Precision %
Cgs(fF)	290	660	300	775	0.4
Cds(fF)	285	370	290	440	0.7
Cgd(fF)	80	37	60	19	1.2
gm(ms)	0	84	0	81	0.5
gd(ms)	0	8	0	6	3

Vgs(V)	-1	0	Precision %
Ri(ohms)	11	2	10

	Rg(Ω)	Rd(Ω)	Rs(Ω)	Lg(pH)	Ld(pH)	Ls(pH)
	1.5	1	1	446	639	2
Precision %	5	9	0.2	0.3	0.4	0.7

The 13 small-signal parameters of the equivalent circuit are determined experimentally by dc and automatic microwave S-parameter (0.1–18 GHz with HP8510) measurements. Special care was taken to define the best initial value of each element in the parameter extraction procedure. We use an optimization program to extract the six constant elements and the seven nonlinear elements as functions of V_{ds} and V_{gs} over the entire frequency range of interest (0.1–18 GHz). Good accuracy is obtained for all model parameters using a three-step procedure: determination of initial parameter values; partial optimization of subsets of parameters in a limited frequency range; and full optimization of parameter extraction in the 0.1–18 GHz range. The modeling routine was applied to three transistors of increasing levels of performance: NEC3SK [10], NEC720, and NEC710. An excellent fit between measured S parameters and those simulated with the model is obtained [11]. Table I presents the data relating to NEC710. The accuracy of extraction is evaluated using a fictitious transistor as in [14]. The small transit time of 2 ps has no apparent influence in the simulations.

The values of all nonlinear elements of the equivalent circuit (Fig. 1(a)) are incorporated directly in 2-D tables (1-D for R_i and I_{gs}) without being expressed analytically. The tables use adjustable voltage increments to describe the variations of each parameter with relatively constant

accuracy over the entire (V_{ds}, V_{gs}) bias range. The increments are 50 mV in the nonlinear regions and 100 mV elsewhere, which for the NEC710 gives 300 bias points. For each calculation time step, the model selects the set of nonlinear parameter values corresponding to the intrinsic dynamic drive voltages across the transistor using a linear interpolation between successive values. At the end of the time step, the new dynamic point is checked for self-consistency with the experimental $I-V$ characteristic. The description of the transistor nonlinearities using 2-D tables combined with simple arithmetic operations provides model accuracy.

The model may be implemented in any time simulator accepting 2-D tables. Only minor modifications are necessary in standard circuit simulators to introduce this feature. The model is incorporated here in the simulator MACPRO [12], which has special capabilities for the CAD of fast circuits with their transmission lines. It may be used in the three basic transistor configurations: common-source, common-drain, and common-gate. There is no restriction on the nature of the load, which is not the usual case in many simulators. Systematic use of the sequential parameter extraction and transfer of numerical data to the tabulated model will be required to implement automatic data transfer.

III. Experimental Setup and Methodology of Simulation

Fig. 1(b) shows the electric circuit of the test card realized in hybrid microstrip technology with a 125-μm-thick Teflon–glass substrate. The packaged NEC710 is mounted in the common-source mode at the center of the circuit. Special precautions were taken to minimize parasitic elements related to transistor fixing on the card, i.e., a direct connection of source to ground metallization. All the passive lumped elements on the card are characterized in the frequency domain with the HP8510 network analyzer and in the time domain by reflectometry (TDR). They are precisely modeled in the simulations.

The response of the whole circuit (PPL generator, card, and attenuator) is measured with the sampling head S4 of a Tek7854 oscilloscope. The step generator of the 7854 (S52 plug-in, 250 mV amplitude, 25 ps rise time) has a 1 V/100 ps slope. It is too slow with too small an amplitude to characterize the intrinsic switching time of a transistor such as the NEC710 in the very large signal regime. The PPL4050A generator (Picosecond Pulse Lab) is more adequate, with a large amplitude ($V_{in}=10$ V on a 50 Ω load) and a fast rise time of $t_m = 50$ ps, which give a much faster response time. With a negative gate bias under threshold V_T, the MESFET does not see the rounded foot of the drive step. The experimental results present the response of the entire system with respective contributions from the PPL generator, the coaxial attenuator, the test card on one side, and the measurement instrumentation S4 sampling head on the other side.

The time-domain simulations are performed with the simulator MACPRO, which easily takes into account transmission line effects [12]. The choice of the substrate and the range of measured switching times on the card (40 ps, see subsection IV-A), allow the dispersion effects in the simulation of transmission lines to be neglected. The responses of each part of the measurement equipment and circuitry are characterized and modeled independently before their introduction in the simulation. The drive step rise time is far from negligible compared to the FET intrinsic switching time and its waveform is described with a numerical table as a function of time.

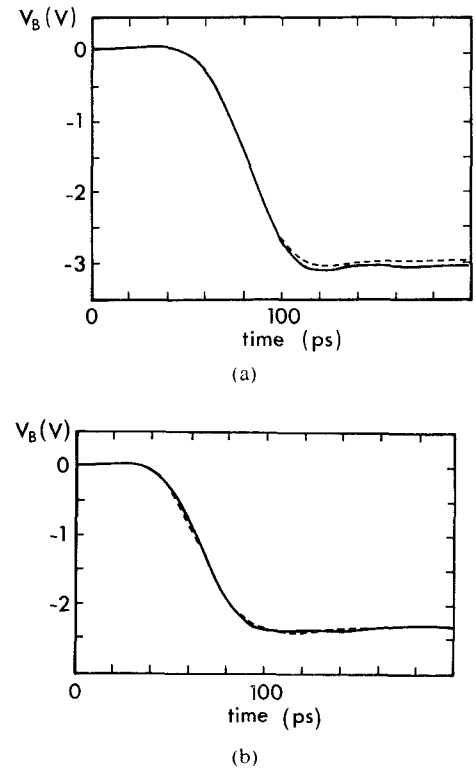

Fig. 2. Measurement (solid lines) and simulation (dotted lines) of the large-signal step response of MESFET NEC710 at point B of Fig. 1(b). Parts (a) and (b) correspond to two different conditions of bias voltage and drive amplitude with the parameters of Table II.

IV. Discussion of Measurements and Simulations of the Step Response

A. Experimental Transistor Response

We present in Fig. 2(a) and (b) two different measurements of the NEC710 strong signal step response. The corresponding bias and drive parameters are shown in Table II. The drain voltage is in the saturation regime for both cases and the gate bias is under threshold. The amplitude of the drive step is adjusted with a wide-band attenuator. It is noticeably larger in Fig. 2(b) than in Fig. 2(a) so that V_{gs} becomes positive and the MESFET Schottky diode strongly clamps the top of the gate signal. This eliminates unwanted reflections due to impedance mismatch and decreases perturbations at the transistor output.

Fig. 2(a) and (b) compares the measured and simulated strong signal responses of the circuit in the time domain and in both cases an excellent agreement is obtained. It

TABLE II
STEP RESPONSE OF MESFET NEC710: PARAMETERS OF THE EXPERIMENTAL MEASUREMENT ILLUSTRATED IN FIG. 2

	Fig. 2(a)	Fig. 2(b)
V_{gs} (V)	−2.25	−1.7
V_{ds} (V)	5.4	3.2
V_{in} (V)	2.3	4.5
measured amplitude (V)	3.11	2.26
simulated amplitude (V)	3.14	2.30
difference (mV)	30	36
switching time 10–90% (ps)	42	36

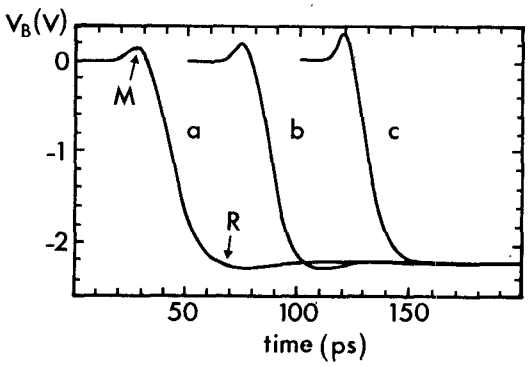

Fig. 3. Simulation of the test card alone (Fig. 1(b)) to determine the NEC710 switching time.

must be emphasized that the simulations do not use any fitting parameters. The wave shapes are very well reproduced in the simulations and the differences in amplitude and switching time between measurement and simulation do not exceed a few percent (Table II). Taking into account the responses of the different instruments, the switching time of the NEC710 may be estimated at this point to be smaller than 25 ps.

B. Determination of the NEC710 Switching Time

The instrumentation has the same order of performance as the NEC710 and therefore does not permit the direct determination of the transistor switching time which is smaller than 25 ps. The reliability of the model shown in subsection IV-A allows an accurate evaluation of the NEC710 intrinsic switching time. We simulate the response of the test card alone driven with a tabulated drive step of 4.5 V amplitude and 5 ps rise time (a rise time variation between 1 and 5 ps has no influence on the simulated response). The response at point B of the test card corresponding to the conditions of Fig. 2(b) is represented in Fig. 3(a). The 10–90 percent switching time of the NEC710 is found to be 20 ± 5 ps. This result is confirmed in a parallel study of the NEC710 as a picosecond sampling gate [15], where a 10–90 percent transition time of the step response $tm = 23 \pm 5$ ps is achieved.

The simulation illustrates the influence of the parasitic elements of the transistor. The resonance at point M when the transistor is still nonconducting is due to direct transmission of the applied signal through C_{gd}/C_{ds}. This phenomenon was clearly observed on a low-speed NEC3SK [10]. In the measured response of the NEC710 (Fig. 2(b)) the time response of the instrumentation is too slow and damps the phenomenon. In the area around point M of the response curve, the parasitic inductance L_g contributes slightly to the resonance but may be barely put into evidence due to the small value of L_g in the NEC710. The inductances L_d and L_s are responsible for the small dip in the response around point R of Fig. 3 when the transistor is conducting. Fig. 3(b) and (c) shows the influence of the parasitic inductances L_g, L_d, and L_s brought by the transistor package. The inductance values in curve b are assumed to be one half of those in curve a and they are neglected in curve c. The dip at point R disappears progressively. The analysis of curves a to c also shows that the parasitic inductances influence the step response. The switching time decreases from Fig. 3(a) to 3(b) but remains approximately constant between Fig. 3(b) and 3(c). In that latter range, the steeper slope of the switching curve is compensated by the rounding of the signal which accompanies the disappearance of the resonance at point R. This illustrates that with very fast transistors, the optimization of the switching time may require an adjustment of the extrinsic parasitic inductances to the device parasitic capacitances.

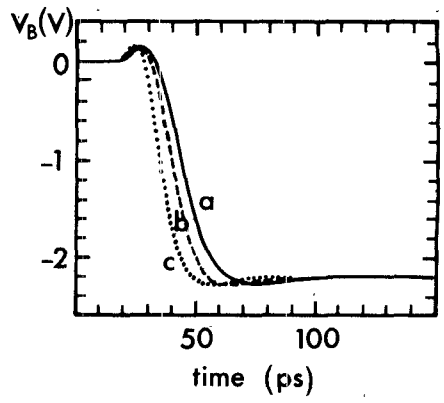

Fig. 4. Influence of transistor description on the accuracy of the transistor step response at point B of Fig. 1(b).

C. Influence of the Description of the Transistor Nonlinearities on the Simulation of Transistor Switching

We now discuss how the description of the transistor nonlinearities affects the accuracy of the transistor time response. The reference is the simulation of Fig. 3(a) reproduced in Fig. 4(a) (switching time 20 ps). In this case all the nonlinear parameters depending on V_{gs} and V_{ds}, i.e., the current sources and the parasitic capacitances, are described by 2-D numerical tables. Curves b and c of Fig. 4 show how a description of nonlinear parameters with averaged values degrades the accuracy of the step response compared with a description using the 2-D tables. The current source I_{ds} is always described by a 2-D table. Curve b corresponds to a description where the three capacitances are represented using a 1-D table as a function of V_{gs}, each value in the table being averaged over the V_{ds} dependence. Here the switching rise time is 16 ps, corresponding to a 20 percent error. Curve c represents a

description where C_{gs} is described with a 1-D table as in curve b and the other capacitances are averaged over their V_{gs} and V_{ds} dependencies. Now the switching time is 13 ps, which means an error of 35 percent. These results emphasize the increasing importance of an accurate description of the nonlinear parameters in time-domain simulation as transistor speeds further increase.

V. Conclusion

A high-accuracy large-signal model of FET's is developed for the time-domain CAD of ultrafast circuits. Numerical 2-D look-up tables describe the nonlinear parameters versus device internal voltages. A dc and microwave FET characterization versus the bias voltages followed by parameter extraction determines completely the parameter tables. The model may be implemented in simulators handling 2-D tables and applied to commercial transistors without a detailed knowledge of their internal technology. The model is validated by the step response of a NEC710 MESFET, demonstrating its accuracy to represent switching waveforms and transient phenomena in the range covering tens of picoseconds. Comparative simulations obtained with some of the nonlinear parameters fixed to average values illustrate the loss in modeling accuracy if the FET nonlinearities are not fully taken into account. The 20 ps switching time of the NEC710 shows that the present methodology of modeling, measurement, and simulation is adequate for studying picosecond transient phenomena in single transistors. The model has been successfully used in the design and analysis of a MESFET sampling gate first with a middle performance transistor NEC3SK [13] and, very recently, with a NEC710 [15].

The methodology of large-signal modeling developed here has great potential for other picosecond transistors such as the heterojunction FET and the heterojunction bipolar transistor.

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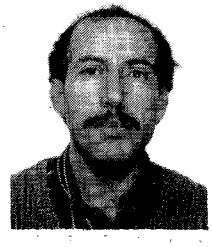

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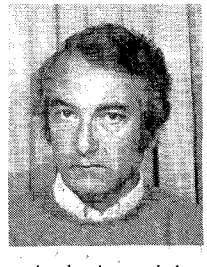

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Robert Adde (M'81–SM'83) obtained the doctorat-es-sciences degree from the Université Paris-Sud, Orsay, in 1966 and spent a postdoctoral year at the Bell Telephone Laboratories, Murray Hill, NJ. He then set up a research group at the Institut d'Electronique. The main activities until 1985 were successively paramagnetic resonance and optical spectroscopies, followed by superconducting Josephson electronics at high microwave frequencies and at picosecond time scales together with far-infrared and mid-infrared laser studies. Since 1984 the activities have turned to III–V semiconductor devices and circuits with special emphasis on modeling, simulation, microwave frequency/picosecond measurements, and, more recently, quantum electronics related to picosecond semiconductor lasers and quantum well/superlattice structures.

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